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1/77

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

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Cardiff Road
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1. Your reference — PAT 99427 GB

2. Patent application number *(The Patent O[redacted]* — 9928574.4

3 DEC 1999

030EC99 E496625-1 D02716
P01/7700 0.00-9928574.4

3. Full name, [redacted] of the or of each applicant *(underline all surnames)*

NOKIA MOBILE PHONES LIMITED
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02150 ESPOO
FINLAND

Patents ADP number *(if you know it)* 59111995004

If the applicant is a corporate body, give the country/state of its incorporation — FINLAND

4. Title of the invention

INTERFACE

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

NOKIA IPR DEPARTMENT
NOKIA HOUSE
SUMMIT AVENUE
FARNBOROUGH
HAMPSHIRE
GU140NG UK

Patents ADP number *(if you know it)* 7577638001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

YES

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Interface

This document describes a proposal for a standard low-pin count RF/BB interface for Bluetooth.

3/7

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The **3-wire data interface** is a dedicated bus for transferring time critical data between the baseband- and the RF-chip in both directions. The needed signals are:

- BBCLK: A synchronization clock for all signals on the data interface. It is generated by the RF-chip. (E.g. 13 MHz for a symbol rate of 1Mbaud @13 fold oversampling). It can also be used as the main clock source for the baseband chip.
- RFBus1: Bidirectional signal between baseband- and RF-chip; usage defined by the respective operating mode.
- RFBus2: Unidirectional signal from baseband- to RF-chip; usage defined by the respective operating mode.

The basic idea is not restricted to 2 data pins It can also be extended to a data interface with more pins if e.g. the data rate is too high for two pins.

Further with a **Sleep-State control signal** "SleepX" the baseband chip is directly able to control the reference oscillator, the power regulators and the default mode of the RF-chip as described later

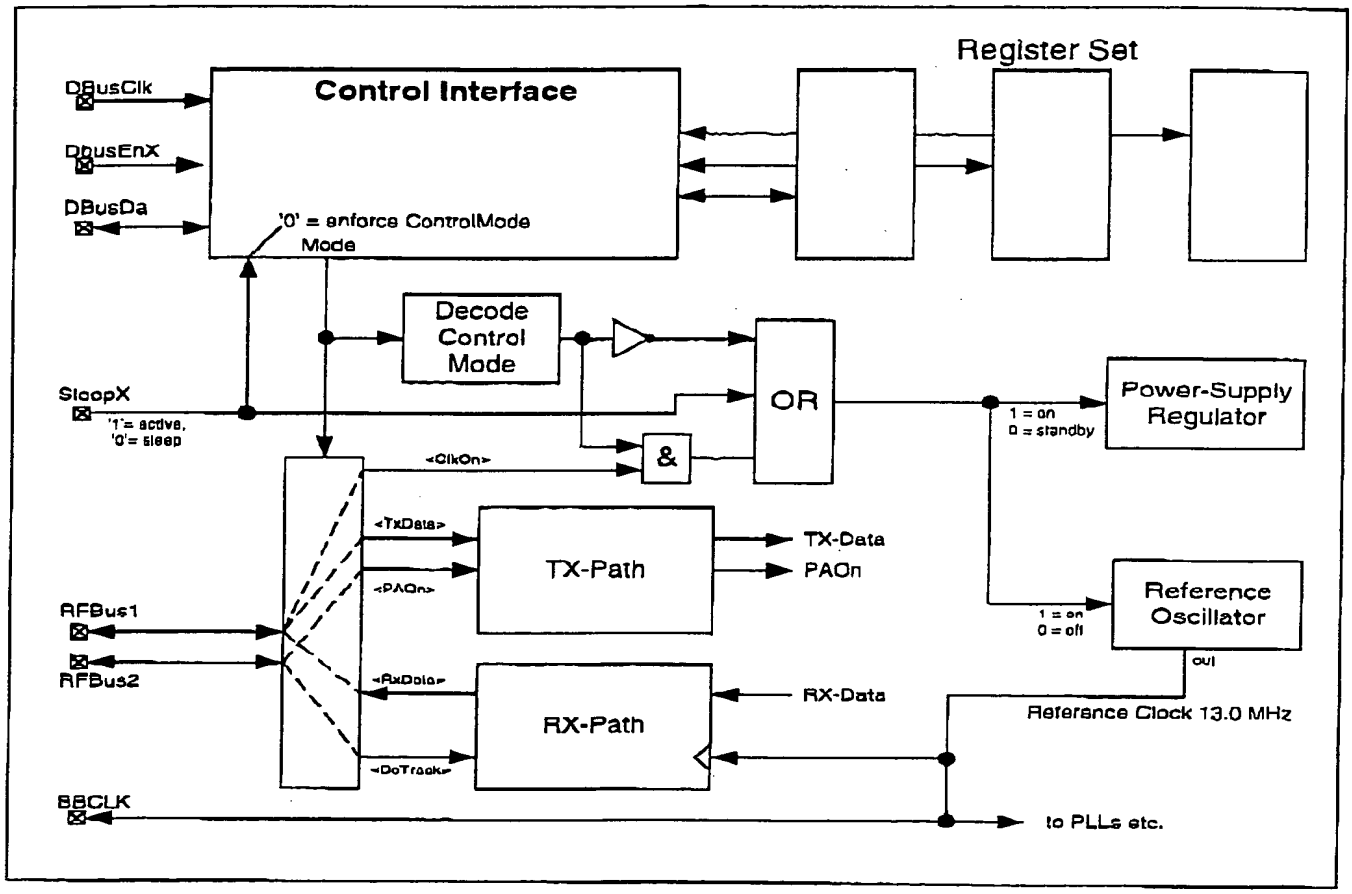

Figure 1: Structure of the Proposed RF-BB-Interface

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5/7

When going to sleep-mode the baseband chip switches off the 13 MHz reference oscillator in order to save power. Further it is able to switch the power regulators to a low quiescent current mode because a sleeping system needs much less power compared to TX or RX.

In the control-mode the **RFBus2** signal is not needed. Therefore the baseband chip fixes the line to '0'.

2.3 The Transmit Mode

After having setup the RF-chip properly during control-mode via the 3-wire control interface (e.g. setting the TX frequency of the synthesizer), a control command sets the mode to TX-Mode.

Then the functionality of the data interface changes. Now the **RFBus1** signal is used for the serial TX-data coming from the baseband chip (functional signal name: "TXDATA").

The **RFBus2** signal is now used for precisely switching on/off the power amplifier of the RF-chip at the time determined by the burst-generator of the baseband chip. The functional signal name now is "PAON".

A synchronization logic on the RF-chip, operating with the low-jitter local reference clock BBCLK can be used to ensure an exact symbol period of the transmitted signal even if the TX-raw-data from the baseband chip exhibits substantial jitter.

2.4 The Receive Mode

During the gap between the TX-burst and Rx-burst the baseband chip reconfigures the RF-chip (e.g. switch the synthesizer to the Rx frequency) and switches to Rx-mode. Here the RF-chip will place the sliced and 13 fold oversampled raw data on the **RFBus1** line for further processing within the baseband chip. BBCLK will be the corresponding oversampling clock.

At the same time the baseband chip will use the **RFBus2** line to aid the DC-estimator within the demodulator (switch between fast acquisition and slow tracking).

3. The Control-Bus Protocol

The 3-wire control bus is a clock, data and enable serial bidirectional interface. The description of the detailed protocol can be found in [1]. It is also possible to use another type of protocol like I^2C ©, as long as the speed is high enough.

One aspect of the present invention relates to a radio transceiver substantially as hereinbefore described with reference to the enclosed drawings and/or as shown in the drawings.

Another aspect of the present invention relates to an interface substantially as hereinbefore described with reference to the enclosed drawings and/or as shown in the drawings.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or implicitly or any generalisation thereof.

Particularly those features listed under the heading 'Aspects of the invention' either singly or in any combination.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made to the foregoing description without departing from the scope of the invention.